

INFORMATION DISCLOSURE STATEMENT BY APPLICANT			Substitute for form 1448A/PTO		Complete if Known	
			Application No.		10/773,385	
			Filing Date		February 5, 2004	
			First Named Inventor		Donald Steiss	
			Art Unit		2127	
			Examiner Name		Not Yet Known	
Sheet	1	of	3	Attorney Docket Number		22347-08564 (Seq. No. 8422)

U.S. PATENT DOCUMENTS				
Examiner Initials*	Cite No. ¹	Document No. Number - Kind Code ² (if known)	Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
cc		US-5,613,114	03-18-1997	Anderson et al.
		US-5,724,586	03-03-1998	Edler et al.
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cc		US-6,507,862	01-14-2003	Joy et al.

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U.S. PATENT DOCUMENTS				
Examiner Initials*	Cite No. ¹	Document No. Number - Kind Code ² (if known)	Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
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		US-6,542,920	04-01-2003	Belkin et al.
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Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶

OTHER REFERENCES – NON-PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ⁶	
EC	C1	Boothe, B. and Ranade, A. G., "Improved Multithreading Techniques for Hiding Communication Latency in Multiprocessors," ACM 1992, pp. 214-223.		
EC	C2	Gulati, M. and Bagherzadeh, N., "Performance Study of a Multithreaded Superscalar Microprocessor," 2 nd International Symposium on High-		

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OTHER REFERENCES – NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		Performance Computer Architecture, February 1996, 11 pages.	
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EL	C4	Tullsen, D. M. et al., "Exploiting Choice: Instruction Fetch and Issue on an Implementable Simultaneous Multithreading Processor," Proc. Of the 23 rd ISCA, May 1996, 12 pages.	
EL	C5	Tullsen, D. M. et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proc. Of the 22 nd ISCA, June 1995, 12 pages.	
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22347/08564/DOCS/1440694.1

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